UD Series

Universal Logic Circuits

Description

The UD series of ULC™s is optimized for conversion of small- to medium-sized PLDs, CPLDs and FPGAs. This series use a unique architecture that provides a high I/O-to-gate ratio. Devices are implemented in high-performance CMOS technology with 0.8-mm (drawn)/0.65-mm (effective) channel lengths, and are capable of supporting flip-flop toggle rates of 200 MHz, operating clock frequencies up to 100 MHz, and input to output delays as fast as 7 ns.

The I/O-intensive architecture of the UD series efficiently supports a conversion of many PLD architecture and FPGA devices types, which would typically result in pad-limited designs with very low core utilization in more traditional gate-array families.

Conversion to the UD series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100 mA or more even when not being clocked. The UD series has a very low standby consumption of 0.4 nA/gate typically, which would yield a standby current of 4 mA on a 10,000 gate design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

With better noise margin at the inputs, and higher drive available on outputs, UD ULCs provide I/O buffers that are better suited for bus interfaces in comparison with FPGAs and PLDs. At the same time, careful latch-up prevention (see section on Technology) completely eliminates the comparative benefits of bipolar technology. Additional safeguards in circuit and technology design afford ESD protection levels in excess of 2000 V.

Features

- High performance ULC™ family suitable for small to medium sized PLDs and FPGAs
- Conversions to approximately 8000 FPGA gates
- Pin counts to 100 pins
- Any pin-out matched due to no dedicated pads
- 0.8-mm (drawn)/0.65-mm (effective) single-layer metal CMOS technology
- Two routing levels in metal and silicide polysilicon
- All inputs incorporate a Schmitt trigger (0.4-V hysteresis) for improved noise immunity
- High current drive capability on each I/O
  - Programmable sink/source current up to 12 mA per buffer (UD10, UD16)
  - Programmable sink/source current up to 24 mA per buffer (UD02, UD03, UD09, UD14, UD27)
  - Up to 48 mA of sink/source current per output pin with parallel output buffers
- Full range of packages: DIPs, SOICs, LCCs/PLCCs, PQFPs/TQFPs, PGAs/PPGAs
- Unique built-in voltage translation allowing mixed voltage operation:
  - 0- to 5-V input voltage allowed on all inputs and I/Os when operating at 3.3 V
  - No input clamping before 7-V Minimum
  - Offers voltage level translation when interfacing between 5-V and 3.3-V logic

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Drive
UD02	31	750	24 mA
UD03	25	800	24 mA
UD09	51	2800	24 mA
UD10	68	3100	12 mA
UD14	78	4100	24 mA
UD16	84	4700	12 mA
UD27	100	8400	24 mA

Architecture

The architecture of the UD series is optimized with: (i) a high I/O-to-gate ratio, (ii) efficient handling of high current outputs, and (iii) high speed at both internal cells and output buffers. All of this is accomplished with the simplicity and reliability of single-layer metal technology.

The I/O-to-gate ratio improvement is achieved through careful I/O placement and gate bank configuration.

Several design considerations support the high-drive capability of the UD Series.

To support the high currents, and to additionally maximize V_{OL} and V_{OH} for better noise margins at the outputs, wide V_{DD} and V_{SS} buses are used on the arrays. These reduce the resistance and thus the IR drop to the outputs.

The configuration of the I/O circuitry is optimized for efficient implementation of TTL-level compatible digital circuits. TTL input level and cell control logic are built in to the I/O without the use of additional core logic for level translation or control logic. I_{OH} is optimized at standard TTL-level V_{OH}, and outputs do not swing rail-to-rail for improved noise margins. As a result, UD series ULCs are not recommended for applications which require CMOS output levels or are driving analog circuitry.

The output buffer transistors are designed such that the output current for each output can be programmed depending on user needs. This enables support of the different current requirements of the different PLD and FPGA types. It can also allow the designer to achieve a higher drive capability than on the original PLD or FPGA for selected pins. In many applications, only a select number of outputs need high-current drive. To eliminate the need for excessive ground bussing, the output buffer can be configured in steps of 6 mA to 24 mA.

Technology

The UD series is unique in the industry in providing small channel lengths and single-layer metal technology. The choice of this technology provides the best available combination of cost and performance for PLD and FPGA conversions.

Single-layer metallization requires only one customization mask. Since mask costs significantly affect minimum order sizes, the single mask required for single-layer metallization makes the UD series the preferred family for ULC conversions up through 100 pins which do not have any special requirements (such as battery back-up) which would dictate the use of another technology.

Historically, the need for dual-layer metal was a function of the intrinsic need for two layers of connections, and the lack of availability of a silicided polysilicon layer for the second connection layer in addition to one layer of metal. Although ordinary polysilicon has been available for such connections and is in fact sometimes used, its resistivity is 500 to 1000 times greater than metal. This prevents its use in high-performance circuits and necessitates dual-layer metal. Silicided polysilicon is roughly 100 times more conductive than ordinary polysilicon and is now available on advanced manufacturing technologies. Although larger devices will require two layers of metal to eliminate the signal skews on long global connections (such as clock signals which would be caused by the interconnect impedance of silicided polysilicon wherever it is used for crossovers), moderate sized devices supported by the UD series do not require two layers of metal due to the small number of crossovers needed.

With single-layer metal technology, excellent routability and utilization are achieved in the UD series through high-density routing channels that are made possible by the dense 0.8-mm technology. An adequate number of routing channels within the cell area allows dense and high-speed intracell connections within macrocells without requiring external routing. A high number of routing channels in the global routing areas further provides easy and efficient inter-macrocell connectivity and thus high performance and high gate utilization. Under certain conditions, routing tracks ordinarily reserved for intracell connections can also be used for intercell connections. Polysilicon connections are only used for short distances across gate banks. The architectural approach of the UD series reduces the need for such connections compared to conventional architectures.

I/O Options

400-mV Schmitt triggers are provided as standard at each input. Outputs can be open collector, tri-state, or internally pulled-up or pulled-down, among many available configurations.

3.3-V Compatibility

Several factors are influencing the growing trend toward 3.3-V circuit operation. Among these are the desire to increase battery operating life, while at the same time decreasing battery weight, improving performance and adding features to notebook and

sub-notebook personal computers. Another is the heat dissipation in ever-denser and faster VLSI semiconductors such as the latest generation of high-performance microprocessor. Despite a growing requirement, a complete complement of 3.3-V system components has been slow to become available.

Moving from 5 V to 3.3 V

In a design such as a notebook PC which typically would not have to accept standard add-in cards, designing for 3.3 V is relatively easy, if all of the desired components are available at 3.3 V. A tougher case would be the design of a desktop machine which must accept existing 5-V add-in cards and in which the mixing of 5-V parts (plentiful, and cheap) and 3.3-V parts (power consumption and noise issues) is desired. Most 3.3-V devices can't stand more than V_{DD} + 0.3 V, creating a problem when interfacing with 5-V parts. Interface logic is required for voltage level translation between 5-V and 3.3-V parts. This interface is a unique capability that the UD Series offers.

A unique CMOS I/O structure

The UD Series I/O structure (Figure 1) has been specifically designed using transistors for input protection instead of the traditional CMOS clamping diodes. Also, the output structure uses an NMOS transistor as a pull-up, instead of the more common PMOS transistor. This allows input signals typically in the 0- to 5-V voltage level range (normal TTL levels are guaranteed), independent of supply voltage with no clamping occurring before the 7-V minimum (Figure 2).

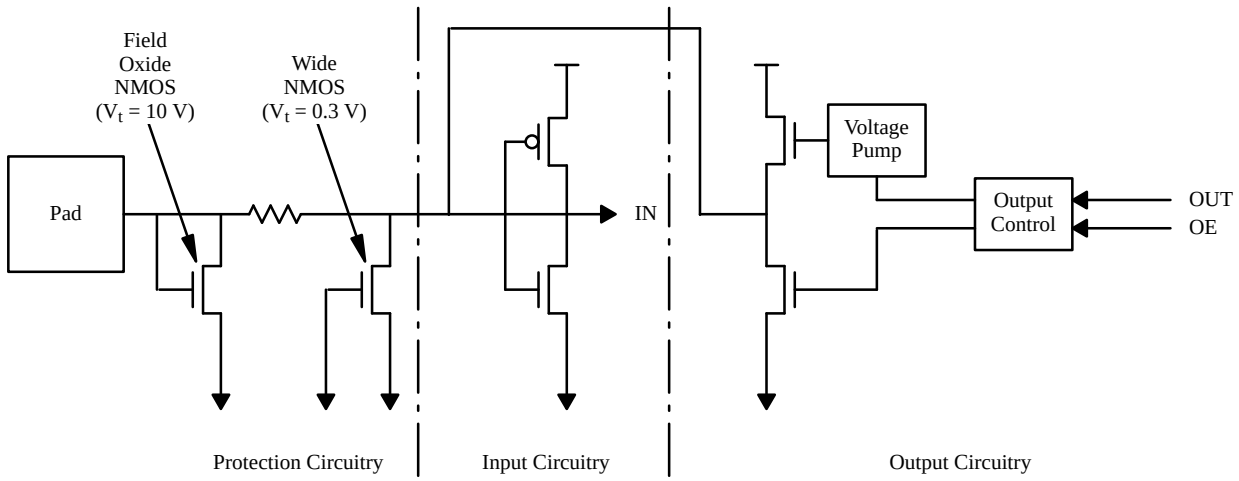

Figure 1. 3-V/5-V Input Compatible I/O Structure

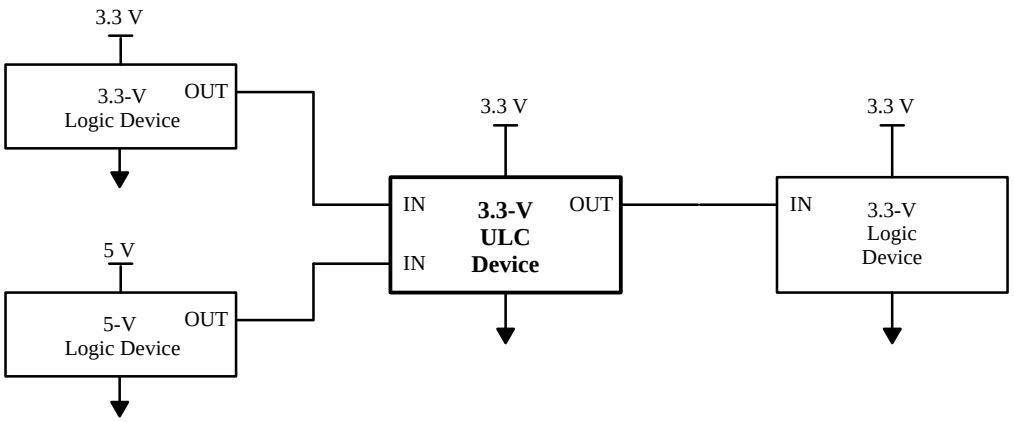

Figure 2. Simple Example of Mixed Power Supply Circuitry

UD Series

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.3 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.3 V to 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

DC Characteristics

Parameter	Symbol	Base Part T_A = Commercial		Min	Typ	Max	Unit
Output Voltage	V_{OH}	V_{DD} = 5 V, I_{OH} (See Note a)		2.4			V
		V_{DD} = 3.3 V, I_{OH} (See Note b)		2.4			
	V_{OL}	I_{OL} (See Note c)				0.5	
Input Voltage	V_{IH}			2.0			
	V_{IL}					0.8	
Input Leakage Current	I_{IX}	$V_{SS} < V_{IN} < V_{DD}$		–10		10	mA
Output Leakage Current	I_{OX}	$V_{SS} < V_{OUT} < V_{DD}$		–10		10	
Output Short Circuit Current	I_{OS}	Buffer Type V_{DD} = 5.25 V	6 mA	–75		75	mA
			12 mA	–150		150	
			16 mA	–200		200	
			24 mA	–300		300	
Dynamic Output Current	I_{OD}		6 mA		0.005		mA/ MHz/ pF
			12 mA		0.01		
			16 mA		0.015		
			24 mA		0.02		
Standby Current	I_{CSB}	V_{DD} = 5.25 V, V_{IN} = V_{SS} Outputs Open	UD02/03/09		1	8	mA
			UD10–27		3	20	
Operating Current	I_{DDINT}				2	5	mA/ Gate/ MHz
Input Capacitance	C_{IN}	V_{DD} = 5.0 V, V_{IN} = 2.0 V				5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 2.0 V				4	

Notes
a. I_{OH} = –rated limit of selected buffer. Selection determined by FPGA or PLD data sheet requirements.
b. I_{OH} = –rated limit of selected buffer. Selection determined by FPGA or PLD data sheet requirements. 3.3-V operation not valid for UD10 and UD16.
c. I_{OH} = rated limit of selected buffer. Selection determined by FPGA or PLD data sheet requirements.

Internal Timing Characteristics

These timing parameters for selected macro cells are provided for information only. Only pin-to-pin timing characteristics are guaranteed for ULCs, and the actual specification is determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed-to separately by MHS.

Conditions: V_{DD} = 5 V, typical Process, Statistical Wire Length. All delays measured at V_{IN}/V_{OUT} = 2.5 V.

Macro Type		Parameter	Symbol	Min	Max (1)[a]	Max (4)[a]	Units
2-Input NAND	NAND2				0.4	0.7	
8-Input NAND	NAND8	Propagation Time	t_{PD}		1.0	1.3	ns
Inverter	INV1				0.5	0.7	
Inverting Tri-State Buffer	TRISTAN				0.5	1.0	

Internal Timing Characteristics (Cont'd)

Macro Type		Parameter	Symbol	Min	Max (1)[a]	Max (4)[a]	Units
Resetable Latch	LATCHRN	Setup Time	t_{SU}	1.5			ns
		Hold Time	t_H	0.0			
		Pulse Width	t_{PW}	2.4			
		Propagation Time	t_{DQ}		0.6	0.7	
		Enable Time	t_{EN}		0.8	1.3	
		Reset Time	t_{RN}		0.3	0.5	
D Flip-Flop with Reset	DFFRN	Setup Time	t_{SU}	1.5			
		Hold Time	t_H	0.0			
		Pulse Width	t_{PW}	2.4			
		Clock Delay Time	t_{CQ}		0.7	1.1	
		Reset Time	t_{RN}		0.7	1.1	
TTL Compatible Input Buffer	BUFINTTL	Propagation Time	t_{PLH}		0.4	0.6	
			t_{PHL}		1.0	1.2	
TTL Compatible I/O Buffer Input Mode	BIOTN4		t_{PLH}		0.4	0.6	
			t_{PHL}		1.0	1.2	
Output Buffer	BON4		t_{PLH}		3.2	8.3	
			t_{PHL}		1.8	2.6	
TTL Compatible I/O Buffer	BIONTN4		t_{PLH}		3.2	8.3	
			t_{PHL}		1.8	2.6	
Tri-State Output Buffer	BIO3N4		t_{PLH}		3.2	8.3	
			t_{PHL}		1.8	2.6	
		Enable Time	t_{PZH}		3.2	8.3	
			t_{PZL}		1.8	2.6	

Notes
a. Fan-outs for internal connection are: FO1 = 1 internal load, F04 = 4 internal loads. Fanouts for output buffers are: F01 = 25 pF, F04 = 100 pF. Max values are provided for worst case of T_{HL} pr T_{LH} for internal cells.

Derating Factors: $t_P = K_P \times K_t \times K_V \times t_{NOMINAL}$

Process												
Process		Best			Nominal			Worst				
K_P		0.75			1.00			1.33				
Ambient Temperature °C												
T_A	–55	–40		0	25		70	85		125		
K_T	0.71	0.76		0.91	1.00		1.16	1.22		1.36		
Supply Voltage												
V_{DD}	3	3.13	3.3	3.47	3.63	4	4.5	4.75	5	5.25	5.5	6
K_V	1.67	1.59	1.5	1.42	1.36	1.22	1.08	1.03	1	0.97	0.96	0.95

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Base Part	Min	Max		Unit
				Typ	Max	
Propagation Time	t_{PD}	UD02		7.0	11.5	ns
		UD03		7.0	11.5	
		UD09		8.0	13.0	
		UD10		8.0	13.0	
		UD14		9.0	14.5	
		UD16		9.0	14.5	
		UD27		10.0	16.0	
Clock Delay Time	t_{CO}	UD02		8.0	13.0	
		UD03		8.0	13.0	
		UD09		10.0	16.0	
		UD10		10.0	16.0	
		UD14		12.0	19.5	
		UD16		12.0	19.5	
		UD27		14.0	22.5	
Hold Time	t_H		0.0			
Output Enable Time	t_{EN}	UD02		8.0	13.0	
		UD03		8.0	13.0	
		UD09		10.0	16.0	
		UD10		10.0	16.0	
		UD14		12.0	19.5	
		UD16		12.0	19.5	
		UD27		14.0	22.5	

Power Consumption

Dynamic Power Consumption for UD Series ULCs

There are four main factors to consider:

1. Static power dissipation of the core is negligible compared to the internal backbias generator pump, so:

   $P_{CSB} = I_{CSB} * V_{DD}$

2. Static power dissipation in I/O buffers:

   $P_1 = V_{OL} * S_n (I_{OLn} * N_{BUFn}) + V_{OH} * S_n(I_{OHn} * N_{BUFn})$

   where:

   N_n is the number of outputs of type n being driven to V_{OL}

   M_n is the number of outputs of type n being driven to V_{OH}

3. Dynamic power dissipation for the internal gates:

   $P_2 = V_{DD} * I_{DDINT} * S_g (N_f * f_g)$

   where:

   N_f = number of gates toggling at frequency f

   f_g = Clock frequency of internal logic in MHz

   Note: A usual rule of thumb is to assume that the average used gate is toggling $^1/_2$-input clock.

4. Dynamic power dissipation in the outputs:

   $P_3 = V_{DD} * S_n (f_n * I_{ODn} * C_n)$

   where:

   f_n = Clocking frequency in MHz of output n

   C_n = Output load capacitance in pF of output n

Global Formula:

$P = P_{CSB} + P_1 + P_2 + P_3$

Example:

We take a 16-bit resettable ripple counter which is approximately 100 gates, operating at a clock frequency of 33 MHz, which gives an average clock frequency of 33 MHz/16 for each bit and each output. There are no static output on this device. Operation is at 5 V, and 6-mA outputs are used and loaded at 25 pF. The output buffers are driving TTL logic, i.e. sinking 24 mA and sourcing a few hundred mA. This is implemented with the UD03 base

$P_{CSB} = 8 * 5 = 40$ mW

$P_1 = 0.4 * 6 * 2 = 0$

$P_2 = 5 * 0.005 * 100 * 33/16 = 5$ mW

$P_3 = 5 * 16 * 33/16 * 0.02 * 25 = 83$ mW

$P = 40 + 0 + 5 + 83 = 128$ mW

Typical ULC Test Conditions

For ac specification purposes, an improved output loading scheme has been defined for MHS high-drive (24 mA), high-speed ULC devices. The schematic below (Figure 1) describes the typical conditions for testing these ULC devices, using the standard loading scheme commonly available on high-end ATE.

Compared to a no-load condition, this provides the following advantages:

- Output load is more representative of “real life” conditions during transitions.

- Transient energy is absorbed at the end of the line to prevent reflections which would lead to inaccurate ATE measurements.

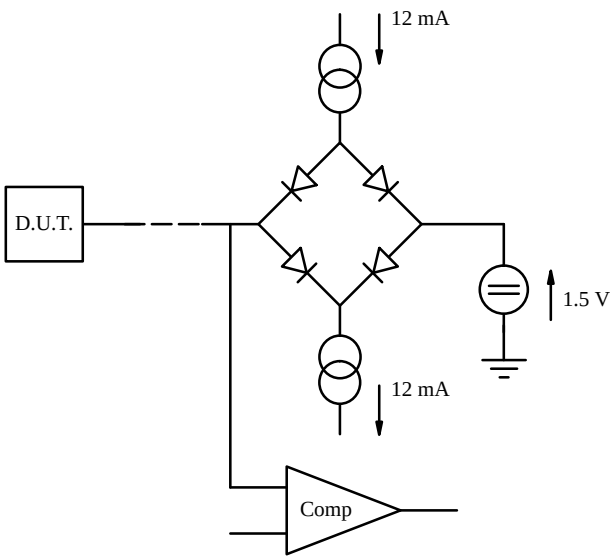

Figure 3. Typical ULC Test Conditions

ULC™ Ordering Information

Prior to conversion, ULCs are referred to by a generic ULC part number and separate package designation plus an optional temperature range formed as follows:

ULC/ *base PLD or FPGA* *pins-package*

where *base PLD or FPGA* refers to 22 V, 10 or EPM7128 or XC3030

Example:
ULC part number for XC3030A-5PL84C would be: ULC/XC3030, 84-PLCC

After conversion, a specific ULC code is ordered as follows:

UC 12 – PQS 160 – MZZ

ULC Series

- **UC** — 0.85-mm, 2-metal CMOS
- **UD** — 0.8-mm, 1-metal CMOS
- **UG** — 0.8-mm, 2- or 3-metal CMOS

Base Matrix

- **UC** — 04, 08, 2, 5, 8, 10, 12, 22, 29, 35, 50, 66
- **UD** — 02, 03, 09, 10, 14, 16, 27
- **UG** — 00, 01, 02, 04, 09, 14, 20, 33, 42, 52, 70, 90, 120, 140, 200

Package

- **PD** — Plastic Dual-In-Line Package (PDIP)
- **SD** — Plastic Skinny Dual-In-Line Package (SDIP)
- **TQ** — Plastic Thin Quad Flatpack—1.4 mm (TQFP)
- **VQ** — Plastic Very-Thin Quad Flatpack—1.0 mm (VQFP)
- **BQ** — Plastic Bumpered Quad Flatpack (BQFP)
- **PL** — Plastic J-Lead Chip Carrier (PLCC)
- **PQS** — Plastic Quad Flatpack with Short Leads (PQFP)
- **PQL** — Plastic Quad Flatpack with Long Leads (PQFP)
- **PP** — Plastic Pin-Grid Array (PPGA)
- **RS** — Plastic Small Outline Package 300-mil (SOIC)
- **SS** — Plastic Small Outline Package 150-mil (SOIC)
- **CD** — Ceramic Dual-In-Line (CDIP)
- **CL** — Ceramic Leadless Chip Carrier (CLCC)
- **CQ** — Ceramic Quad Flatpack (CQFP)
- **CP** — Ceramic Pin-Grid Array (CPGA)
- **CJ** — Ceramic J-Lead Chip Carrier (CLCCJ)

Pin Count
Number of Pins

Pattern
Unique Customer Pattern Code